Y1 – S1 CLASS TIME TABLE

(17th February 2025) to (30th May 2025)

Semester Final Written Examinations: 10th and 11th June 2025

Start Time	Monday	Tuesday	Wednesday	Thursday	Friday
9.30 am - 12.30 pm		Digital Electronics **(Lec)**	Engineering Circuit Analysis **(Lec)**	Engineering Mathematics I **(Lec)**	Professional Practice and the Environment I **(Lec + Lab)**
BREAK					
1.00 pm - 4.00 pm	Programming Fundamentals **(Lec + Lab)**	Digital Electronics **(Lab)**	Engineering Circuit Analysis **(Lab)**	Engineering Mathematics I **(Lab)**	Tutorial Sessions **(ECA&DE)**

Lecture Hall: 12th Floor Hall No 3

Laboratory: 7th Floor Electronic/Electrical Laboratory

Module Code and Title	Lecturers in Charge
EE060101 - Engineering Mathematics I	Mr. Lawrence Jerith
EE060102 - Engineering Circuit Analysis	Mr. Lawrence Benorith
EE060103 - Digital Electronics	Prof. Indra Dayawansa
EE060104 - Programming Fundamentals	Mr. Lawrence Benorith
EE060105 - Professional Practice and the Environment I	Mr. Joseph Lakshan